FORM PTO-1390 (REV 10-2000) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER: FRR-12671

U.S. APPLICATION NO. (If known, see 37 CFR 1.5): 09/936962

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/EP00/02404	17 March 2000	19 March 1999

TITLE OF INVENTION: MULTI-CHIP MODULE

APPLICANT(S) FOR DO/EO/US: STEIERT, Philippe; STAUFERT, Gerhard

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. [X] This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. [ ] This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. [ ] This is an express request to promptly begin national examination procedures (35 U.S.C. 371(f)).
4. [X] The US has been elected by the expiration of 19 months from the priority date (PCT Article 31).
5. [X] A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. [ ] is attached hereto (required only if not communicated by the International Bureau).
   b. [X] has been communicated by the International Bureau.
   c. [ ] is not required, as the application was filed in the United States Receiving Office (RO/US).
6. [X] An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
7. [X] Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. [ ] are attached hereto (required only if not communicated by the International Bureau).
   b. [ ] have been communicated by the International Bureau.
   c. [ ] have not been made; however, the time limit for making such amendments has NOT expired.
   d. [X] have not been made and will not be made.
8. [ ] An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. [ ] An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. [ ] An English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 16 below concern document(s) or information included:

11. [ ] An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. [ ] An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. [X] A FIRST preliminary amendment.
    [ ] A SECOND or SUBSEQUENT preliminary amendment.
14. [ ] A substitute specification.
15. [ ] A change of power of attorney and/or address letter.
16. [X] Other items or information:

    Application Data Sheet.

U.S. APPLICATION NO. (if known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO	ATTORNEY'S DOCKET NUMBER
09/936962	PCT/EP00/02404	FRR-12671

17. ☒ The following fees are submitted:

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :

Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO **$1000.00**

International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO **$860.00**

International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO **$710.00**

International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4) **$690.00**

International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4) **$100.00**

	CALCULATIONS PTO USE ONLY	
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 860.00	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☒ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$ 130.00	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	20 - 20 =	0	X **$18.00**	$ 0.00	
Independent claims	2 - 3 =	0	X **$80.00**	$ 0.00	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ **$270.00**	$ 0.00	
TOTAL OF ABOVE CALCULATIONS =				$ 990.00	
☑ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.				$ 495.00	
SUBTOTAL =				$ 495.00	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☒ 30 months from the earliest claimed priority date (37 CFR 1.492(f)). +				$ 0.00	
TOTAL NATIONAL FEE =				$ 495.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +				$ 0.00	
TOTAL FEES ENCLOSED =				$ 495.00	
				Amount to be refunded:	$
				charged:	$

a. ☒ A check in the amount of $ 495.00 to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. 18-0160 in the amount of $_____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 18-0160. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Customer No. 007609
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SIGNATURE:

David E. Spaw
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34732
REGISTRATION NUMBER

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Philippe Steiert and Gerhard Staufert
Serial No.:	N/A
Art Unit:	N/A
Filing Date:	Herewith
International Application No.:	PCT/EP00/02404
International Filing Date:	17 March 2000
Title:	MULTI-CHIP MODULE
Examiner:	N/A
Docket No.:	FRR-12671

PRELIMINARY AMENDMENT "A"

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Please amend the above-identified application, prior to examination thereof, in the following manner.

Express Mail Label No.: EL653252118US

IN THE CLAIMS:

Please amend the claims as follows:

1. (Amended) A multi-chip-module with a base carrier (1), on which at least in some areas signal conductor tracks (2, 8) arranged at least in a single layer and signal contact surfaces (4) are arranged, and with at least one semiconductor component (11) connected with signal conductor tracks (2) and signal contact surfaces (4) operating in the signal range, wherein additionally on the base carrier (1) at least in some areas power conductor tracks (5) and power contact surfaces (7, 7a) are arranged in at least a single layer, at least one power electronics component (12) operating in the power range is provided, which is connected with at least one power conductor track (5), at least one power contact surface (7, 7a) and at least one signal conductor track (2, 8) and the power conductor tracks (5) have a larger cross section than the signal conductor tracks (2) at least on the basis of greater thickness dimensions.

2. (Amended) The multi-chip-module in accordance with claim 1, wherein the at least one signal conductor track (2, 8) leading to a power electronics component (12) essentially seamlessly verges into a power conductor track (5) and/or power contact surface (7).

3. (Amended) The multi-chip-module according to claim 1, wherein the ratio of the height of a power conductor track (5) and/or power contact surface (7, 7a) to the signal conductor track (2,8) and/or signal contact surface (4) is situated within the range of 2 to 300, in preference 120 to 130.

4. (Amended) The multi-chip-module according to claim 1, wherein the ratio of the conductor cross section of a power conductor track (5) and/or power contact surface (7, 7a) to the conductor cross section of a signal conductor track (2, 8) amounts to 2 to 1000, in preference 80 to 400.

5. (Amended) The multi-chip-module according to claim 1, wherein the ratio of height to width of a power conductor track (5) and/or power contact surface (7, 7a) is situated in the range of 0.1 to 10, in preference 1 to 4.

6. (Amended) The multi-chip-module according to claim 1, wherein at least one power conductor track (5) merges into several power contact surfaces (7a) for the common contacting of a power electronics component (12).

7. (Amended) The multi-chip-module according to claim 1, wherein signal connection contact surfaces (3) and power connection contact surfaces (6) are provided for an external connection belonging to them, wherein the signal connection contact surfaces (3) and the power connection contact surfaces (6) essentially are of the same height.

8. (Amended) The multi-chip-module according to claim 1, wherein signal connection contact surfaces (3) and power connection contact surfaces (6) are arranged on the side of the base carrier (1), which is opposite the semiconductor components (11) and power electronics components (12) (reverse side), wherein the connection contact surfaces (3, 6) are electrically in connection with the opposite side (front side) by means of conductor track sections passing through the base carrier (1).

9. (Amended) The multi-chip-module according to claim 1, wherein the dimension, which results from the height of a power conductor track (5) minus the height of a power contact surface (7a) electrically in connection with this power conductor track (5), is either the same or greater than the height of the power electronics component (12) contacting this power contact surface (7a).

10. (Amended) The multi-chip-module according to claim 1, wherein on the base carrier (1) at least one heat conducting element is jointly arranged, which is in a thermally conducting connection with a power electronics component (12).

11. (Amended) The multi-chip-module according to claim 10, wherein the at least one heat conducting element (9) is connected with a heat exchanger device (13).

12. (Amended) The multi-chip-module according to claim 11, wherein the heat exchanger device (13) is located on the reverse side of the base carrier (1) and the heat conducting element (9) passes through the base carrier (1).

13. (Amended) The multi-chip-module according to claim 11, wherein the heat exchanger device (13) comprises fine cooling ribs with a ratio of height to width of 0.1 to 10, in preference 1 to 4.

14. (Amended) The multi-chip-module according to claim 1, wherein a heat exchanger device (13) is directly thermally conductively connected with a power electronics component (12).

15. (Amended) The multi-chip-module according to claim 1, wherein the signal connection contact surfaces (3) and the power connection contact surfaces (6) are grouped and arranged on the base carrier (1) in such a manner, that the module is capable of being inserted into a standardised base.

16. (Amended) A method for manufacturing a multi-chip-module, comprising the steps of:

preparing a base carrier (1) with signal conductor tracks (2, 8) and signal contact surfaces (4),

depositing a structured layer, by which at least the signal conductor tracks (2) and signal contact surfaces (4) are essentially covered with the exception of connection points and which comprises a negative structure of the power conductor tracks (5) and/or power contact surfaces (7, 7a),

filling-up of the negative structure by means of a metallisation process for the creation of the power conductor tracks (5) and/or power contact surfaces (7), wherein at the connection points a contacting of the signal conductor tracks (2, 8) and/or signal contact surfaces (4) and of the power conductor tracks (5) and/or the power contact surfaces (7) is effected.

17. (Amended) The method according to claim 16, wherein a conductive adhesive layer is deposited on the base carrier (1) in the zone of the negative structure, which serves as base for the metallisation process.

18. (Amended) The method according to claim 16, wherein the structured layer is deposited by means of a photo-lithographic process.

19. (Amended) The method according to claim 16, wherein the metallisation process is effected by the galvanic deposition of metal.

20. (Amended) The method according to claim 19, wherein, following the metallisation process, the structured layer is removed.

IN THE ABSTRACT:

Please replace the original abstract with the following new abstract of the disclosure:

ABSTRACT OF THE DISCLOSURE

A multi-chip-module includes a base carrier on which signal conductor tracks and signal contact surfaces arranged at least in a single layer are located, and with a semiconductor component operating in the signal range and connected with the signal conductor track and signal contact surfaces. A high degree of integration is achieved with a multi-chip-module of this type. In some areas on the base carrier power conductor tracks and power contact surfaces arranged in at least one layer are located. Furthermore, at least one power electronics component, operating in the power range, is provided, which is connected with at least one power conductor track, at least one power contact surface and at least one signal conductor track. The power conductor tracks have a larger cross section than the signal conductor tracks at least on the basis of greater thickness dimensions.

REMARKS

Attached hereto is a marked-up version of the changes made to the application by the present Amendment. If clarification of the amendment or application is desired, or if issues are present which the Examiner believes may be quickly resolved, the Examiner is invited to initiate a telephone interview with the undersigned attorney to expedite prosecution of the present application.

If there are any additional fees resulting from this communication, please charge same to our Deposit Account No. 18-0160, our Order No. FRR-12671.

Respectfully submitted,

RANKIN, HILL, PORTER & CLARK LLP

By: _____
David E. Spaw, Reg. No. 34732

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Attachment: Marked-up version of Amendments

Marked-up Version of Amendment

IN THE CLAIMS:

The claims have been amended as follows:

1. (Amended) ~~[Multi]~~ A multi-chip-module with a base carrier (1), on which at least in some areas signal conductor tracks (2, 8) arranged at least in a single layer and signal contact surfaces (4) are arranged, and with at least one semiconductor component (11) connected with signal conductor tracks (2) and signal contact surfaces (4) operating in the signal range, ~~[characterised in that]~~ wherein additionally on the base carrier (1) at least in some areas power conductor tracks (5) and power contact surfaces (7, 7a) are arranged in at least a single layer, at least one power electronics component (12) operating in the power range is provided, which is connected with at least one power conductor track (5), at least one power contact surface (7, 7a) and at least one signal conductor track (2, 8) and the power conductor tracks (5) have a larger cross section than the signal conductor tracks (2) at least on the basis of greater thickness dimensions.

2. (Amended) ~~[Multi]~~ The multi-chip-module in accordance with claim 1, ~~[characterised in that]~~ wherein the at least one signal conductor track (2, 8) leading to a power electronics component (12) essentially seamlessly verges into a power conductor track (5) and/or power contact surface (7).

3. (Amended) ~~[Multi]~~ The multi-chip-module according to claim 1 ~~[or 2, characterised in that]~~, wherein the ratio of the height of a power conductor track (5) and/or power contact surface (7, 7a) to the signal conductor track (2,8) and/or signal contact surface (4) is situated within the range of 2 to 300, in preference 120 to 130.

4. (Amended) ~~[Module in accordance with one of the claims 1 to 3, characterised in that]~~ The multi-chip-module according to claim 1, wherein the ratio of the conductor cross section of a power conductor track (5) and/or power contact surface (7, 7a)

to the conductor cross section of a signal conductor track (2, 8) amounts to 2 to 1000, in preference 80 to 400.

5. (Amended) ~~[Module]~~ The multi-chip-module according to ~~[one of the claims 1 to 4, characterised in that]~~ claim 1, wherein the ratio of height to width of a power conductor track (5) and/or power contact surface (7, 7a) is situated in the range of 0.1 to 10, in preference 1 to 4.

6. (Amended) ~~[Module in accordance with one of the claims 1 to 5, characterised in that]~~ The multi-chip-module according to claim 1, wherein at least one power conductor track (5) merges into several power contact surfaces (7a) for the common contacting of a power electronics component (12).

7. (Amended) ~~[Module]~~ The multi-chip-module according to ~~[one of the claims 1 to 6, characterised in that]~~ claim 1, wherein signal connection contact surfaces (3) and power connection contact surfaces (6) are provided for an external connection belonging to them, wherein the signal connection contact surfaces (3) and the power connection contact surfaces (6) essentially are of the same height.

8. (Amended) ~~[Module in accordance with one of the claims 1 to 7, characterised in that]~~ The multi-chip-module according to claim 1, wherein signal connection contact surfaces (3) and power connection contact surfaces (6) are arranged on the side of the base carrier (1), which is opposite the semiconductor components (11) and power electronics components (12) (reverse side), wherein the connection contact surfaces (3, 6) are electrically in connection with the opposite side (front side) by means of conductor track sections passing through the base carrier (1).

9. (Amended) ~~[Module]~~ The multi-chip-module according to ~~[one of the claims 1 to 8, characterised in that]~~ claim 1, wherein the dimension, which results from the height of a power conductor track (5) minus the height of a power contact surface (7a) electrically in

connection with this power conductor track (5), is either the same or greater than the height of the power electronics component (12) contacting this power contact surface (7a).

10. (Amended) ~~[Module in accordance with one of the claims 1 to 9, characterised in that]~~ The multi-chip-module according to claim 1, wherein on the base carrier (1) at least one heat conducting element is jointly arranged, which is in a thermally conducting connection with a power electronics component (12).

11. (Amended) ~~[Module]~~ The multi-chip-module according to claim 10, ~~[characterised in that]~~ wherein the at least one heat conducting element (9) is connected with a heat exchanger device (13).

12. (Amended) ~~[Module in accordance with]~~ The multi-chip-module according to claim 11, ~~[characterised in that]~~ wherein the heat exchanger device (13) is located on the reverse side of the base carrier (1) and the heat conducting element (9) passes through the base carrier (1).

13. (Amended) ~~[Module]~~ The multi-chip-module according to claim 11 ~~[or 12, characterised in that]~~, wherein the heat exchanger device (13) comprises fine cooling ribs with a ratio of height to width of 0.1 to 10, in preference 1 to 4.

14. (Amended) ~~[Module in accordance with one of the claims 1 to 13, characterised in that]~~ The multi-chip-module according to claim 1, wherein a heat exchanger device (13) is directly thermally conductively connected with a power electronics component (12).

15. (Amended) ~~[Module]~~ The multi-chip-module according to ~~[one of the claims 1 to 14, characterised in that]~~ claim 1, wherein the signal connection contact surfaces (3) and the power connection contact surfaces (6) are grouped and arranged on the base carrier (1) in such a manner, that the module is capable of being inserted into a standardised base.

16. (Amended) [Method] A method for [the manufacture of] manufacturing a multi-chip-module [with], comprising the [following] steps of: preparing[:Preparation of] a base carrier (1) with signal conductor tracks (2, 8) and signal contact surfaces (4),

[deposition of] depositing a structured layer, by which at least the signal conductor tracks (2) and signal contact surfaces (4) are essentially covered with the exception of connection points and which comprises a negative structure of the power conductor tracks (5) and/or power contact surfaces (7, 7a),

filling-up of the negative structure by means of a metallisation process for the creation of the power conductor tracks (5) and/or power contact surfaces (7), wherein at the connection points a contacting of the signal conductor tracks (2, 8) and/or signal contact surfaces (4) and of the power conductor tracks (5) and/or the power contact surfaces (7) is effected.

17. (Amended) [Method] The method according to claim 16, [characterised in that] wherein a conductive adhesive layer is deposited on the base carrier (1) in the zone of the negative structure, which serves as base for the metallisation process.

18. (Amended) [Method in accordance with claim 16 or 17, characterised in that] The method according to claim 16, wherein the structured layer is deposited by means of a photo-lithographic process.

19. (Amended) [Method] The method according to [one of the claims 16 to 18, characterised in that] claim 16, wherein the metallisation process is effected by the galvanic deposition of metal.

20. (Amended) [Method in accordance with] The method according to claim 19, [characterised in that] wherein, following the metallisation process, the structured layer is removed.

IN THE ABSTRACT:

The Abstract of the Disclosure has been amended as follows:

[Abstract] ABSTRACT OF THE DISCLOSURE

[The invention is related to a multi-chip-module and to a method for its manufacture. The module comprises a base carrier, on which at least in some areas] A multi-chip-module includes a base carrier on which signal conductor tracks and signal contact surfaces arranged at least in a single layer are located, and with [at least one] a semiconductor component operating in the signal range and connected with the signal conductor track and signal contact surfaces. [The purpose is to achieve a] A high degree of integration is achieved with a multi-chip-module of this type. [To do so, in addition at least in] In some areas on the base carrier power conductor tracks and power contact surfaces arranged in at least one layer are located. Furthermore, at least one power electronics component, operating in the power range, is provided, which is connected with at least one power conductor track, at least one power contact surface and at least one signal conductor track. The power conductor tracks have a larger cross section than the signal conductor tracks at least on the basis of greater thickness dimensions.

MULTI-CHIP-MODULE

The invention presented here relates to a multi-chip-module with a base carrier, on which at least in some areas signal conductor tracks and signal contact surfaces are arranged in a single layer, and with at least one semiconductor component operating in the signal range connected with signal conductor tracks and signal contact surfaces.

Multi-chip-modules (MCM) in prior art serve for the highly integrated arrangement of semiconductor components operated in the signal range (i.e., computer components, memory components, I-O components, etc.). MCMs of this type comprise very fine structures of conductor tracks and contact surfaces, wherein semiconductor components mostly present in the form of unhoused chips are in connection with the contact surfaces. Several of these semiconductor components are arranged on a common base carrier. Within the technology, a series of differing designs of such MCMs exist, mentioned as examples shall be solely the EP 0871222 A2, WO 97/22138, WO 97/20273 and EP 0856888 A2. Multi-chip-modules of this type, e.g., are arranged on printed circuit boards and contacted through corresponding supply lines of the printed circuit board. Common to all known MCMs, however, is that they exclusively relate to the combination of digital and/or analogue semiconductor components, which are operated with electric powers in the signal range and which as a rule are utilised for the outputting of control signals. The conductor tracks and contact surfaces have a small cross section and can be arranged in a single layer or multilayered on a suitable carrier material, so that depending on the case in question a structure in the sense of an MCM-L, an MCM-C or an MCM-

D is present. These types designated in such a manner in the specialist literature differ from one another with respect to the carrier material and the lateral density of the electrically conductive structure. With these conductor tracks and contact surfaces of small cross section, the desired signal semiconductor components, which can be present as unhoused chips or as „chip-packed devices" or as SMD component, etc., are capable of being contacted. MCMs of this type are also utilised for the controlling of semiconductor components with electric powers from a few Watts to some kilowatts, in that electric control signals with a low power are applied to corresponding inputs of these semiconductor components. In the fields of the controlled electric power supply of medium to high power, e.g., in the case of small electric motors, electro-pneumatic modules, motors for machine tools, motors for automobiles and right through to locomotive motors, no complete electric isolation of signal circuit and power circuit has to be present.

In other fields of application, e.g., in telecommunications, a strict electric isolation of the driving primary circuit from the secondary circuit conducting the electric power is demanded. In such a case, electronic components, such as switching relays, reed relays, etc., are employed, which on the basis of more recent developments are becoming smaller and smaller in their dimensions.

In particular in the field of small automatic units (small robots, automatic assembly units, etc.), also, however, in the field of telecommunications, it has proved to be a problem, that the electronic structures necessary for the operation of the unit, still have a disruptively large volume and that on the other hand the operational reliability is limited by the terminals, plugs and other devices for creating electric contact between two structurally independent components.

The invention is therefore based on the objective of making available a highly integrated circuit layout in the case of an MCM of the type mentioned at the beginning.

This objective is achieved in the case of a multi-chip-module mentioned at the beginning by the fact, that in addition on the base carrier at least in some areas power conductor tracks and power contact surfaces arranged in a single-layer are provided, at least one power electronics component operating in the power range is provided, which is connected with the at least one power conductor track, at least one power contact surface and at least one signal conductor track, and that the power conductor tracks have a larger cross section that the signal conductor tracks at least on the basis of greater thickness dimensions. The comparison of cross sections preferably shall not be referred to the overall cross section of all conductor tracks, but shall be referred to the individual cross section of the respective conductor track.

While from the printed circuit board technology it is known how to equip a base carrier with a conductive layer and subsequently by means of photo-lithography to create a conductor track structure on this carrier, wherein conductors of differing cross sections can be produced by differing conductor track widths, this process, however, cannot be transferred to the production of very much smaller and for this reason very much more finely structured MCMs. Because of the excessive widening of conductor tracks for the purpose of obtaining a suitable cross section, the high integration on an MCM would not be implementable.

In contrast to this, in accordance with the invention it is proposed to arrange power electronics components, which in the meantime are also available in small format, which are operated with a much higher power than the signal semiconductor

components, on one and the same base carrier as the signal control system. This is implemented by conductor tracks with a greater thickness than the respectively thinner signal conductor tracks. By means of this, the power conductor tracks can also be arranged very close together, as a result of which the high integration can take place on the common base carrier. In addition, the integration of driving electronics and power electronics on an MCM provides the opportunity to offer the users „intelligent power electronics components". Therefore on the same carrier in addition to the conductors with a small cross section, conductors and contact surfaces with a large cross section are present, by means of which the required power electronics components (power semiconductors, relays, etc.) can be contacted. From the zone with the conductors of a small cross section, special conductors lead into the zone with conductors with a large cross section, which are able to transmit the corresponding control signals between the signal semiconductor and the power semiconductors. With this, in the smallest possible space and without any connecting elements susceptible to malfunction a driving of the power electronics components with signal semiconductors is implemented.

Furthermore, there is the possibility, that the at least one signal conductor track leading to a power electronics component essentially seamlessly verges into a power conductor track and/or power contact surface. If the same materials are utilised for the power electronic conductor tracks and the signal conductor tracks, then on the basis of suitable manufacturing methods a tight bond of these conductor tracks is produced, which is superior to all other contacting methods. The control signal therefore can be transmitted to the power electronics components with the utmost precision and without any interference. Connecting elements susceptible to malfunction, such as solder points, are therefore superfluous.

Methods mastered up until now have shown, that the ratio of the height of a power conductor track and/or power contact surfaces to the height of a signal conductor track and/or signal contact surface is situated within the range of 2 to 300, preferably in a ratio of 20 to 180. On the basis of such a significant difference it is possible to throughput much higher powers through the power conductor tracks than through the signal conductor tracks, without a large lateral space being required for different power conductor tracks or power contact surfaces.

In preference, in this context the ratio of conductor cross section of power conductor track and/or power contact surface to the conductor cross section of a signal conductor track may amount to 2 to 1000, in preference 80 to 400. Here too, it becomes clear, that on the basis of the enormously enlarged cross section the power capacity differences of the conductor tracks in the signal range and in the power range can be considerable.

An also preferred ratio of height to width of a power conductor track and/or power contact surface in the case of one embodiment is situated in the range of 0.1 to 10, preferably 1 to 4. By means of a combination of widening and increasing the height of the power conductor track relative to the signal conductor tracks, a compromise is achieved, which contributes decisively to the high integration on a common base carrier.

In most cases it can be foreseen, that at least one power conductor track merges into several power contact surfaces for the purpose of jointly contacting a power electronics component. This signifies, that this conductor track comprises branches (junctions) corresponding to the number of contact surfaces. If the power is

distributed over the individual contact surfaces, then these can have a correspondingly smaller cross section.

In order for the MCM to be able to be electrically connected to the outside, in accordance with a further embodiment signal connection contact surfaces and power connection contact surfaces for a respective external connection are provided, wherein the signal connection contact surfaces and the power connection contact surfaces essentially have the same height. As a result of the same height of these contact surfaces, the layout of the MCM is facilitated, because the contact surfaces additionally can be utilised for the positioning. In the case of correspondingly high contact surfaces, the MCM can be installed head first, so that the components arranged on the base carrier are automatically protected.

Another procedure for the equalisation of the differing heights of signal conductor tracks and power conductor tracks consists in arranging the signal contact surfaces and the power contact surfaces on the side opposite the semiconductor components and power electronics components (reverse side) of the base carrier, wherein the connection contact surfaces are in electrical connection with the opposite side (front side) through the conductor track sections, which pass through the base carrier. On the reverse side of the base carrier, the contact surfaces then can have a relatively low height independent of the height of the conductor tracks arranged on the front side, wherein the power contact surfaces are designed correspondingly larger. This, however, because of the space conditions prevailing on the reverse side does not prove to be a disadvantage.

An adequate protection for the power electronics components as well as a relatively flat construction height can be achieved by the value, which results from the height

of a power conductor track minus the height of a contact surface in electrical contact with this power conductor track, being the same or greater than the height of the power electronics component contacting this power contact surface. This signifies, that the power conductor tracks protectively surround the electronic components and, because they are higher than them, provide a protection against shocks.

A further important aspect, which is important in the case of an integration of signal circuits and power circuits on an MCM, consists in the adequate heat dissipation. For this purpose it is possible to assure, that at least one heat conducting element is provided on the base carrier, which is in a thermally conductive connection with a power electronics component. This heat conducting element then conducts the superfluous heat away from the power electronics component, which thereupon can be dissipated through it in any suitable form.

For this purpose, provisions additionally can favourably be made, that at least one heat conducting element is connected with a heat exchanger device. The heat exchanger device then takes care of the corresponding dissipation of the heat in function of the power of the electronics component. Possible as heat exchanger devices are all means in miniature form suitable for this purpose, independent of whether a forced cooling or anything similar is provided. In order to also not excessively burden the front side of the MCM with the heat exchanger equipment, so that a high degree of integration is not impaired by this, it may also be arranged on the reverse side of the base carrier, wherein the heat conducting element passes through the base carrier. The heat conducting element therefore conducts the heat through the base carrier to the heat exchanger device arranged on the reverse side. This has advantages in particular in the case of MCMs installed head first, because the possibly tight installation conditions do not lead to a build-up of heat, because the heat is conducted into regions, where an adequate heat exchange can be provided for.

In the case of a variant of the heat exchanger it is foreseen, that it comprises fine cooling ribs with a ratio of height to width of 0.1 to 10, in preference 1 to 4. Cooling ribs of this type are capable of being manufactured in a similar manner as the conductor tracks and therefore they have a relatively large ratio of height to width. This with relatively small structures makes it possible to provide very high heat exchange rates.

A further variant consists in the fact, that a heat exchanger device is connected with a power electronics component in an immediately thermally conductive manner. A cooling structure of this kind can be directly mounted on the power electronics components by means of correspondingly suitable mans of connection, e.g., a thermally conductive adhesive.

In order to be in a position to assure a standardisation, in accordance with an embodiment provisions are made, that the signal contact surfaces and the power contact surfaces are arranged grouped on the base carrier in such a manner, that the module can be inserted into a standardised base. Here there is also the possibility of grouping the contact surfaces in such a way, that bases, which are already present, can be utilised. These then solely have to have suitable contacts at the corresponding points for the connection of the power circuits.

The invention furthermore is related to a method for the manufacture of a multi-chip-module. The method comprises the following steps:

Preparation of a base carrier with signal conductor tracks and signal contact surfaces, deposition of a structured layer, by which at least the signal conductor tracks and

signal contact surfaces are essentially covered except for connection points and which comprises a negative structure of the power conductor tracks and/or power contact surfaces.

Filling in the negative structures by means of a metallisation process for the creation of the power conductor tracks and/or contact power surfaces, wherein at the connection points a contacting of the signal conductor tracks and/or of the signal contact surfaces and of the power conductor tracks and/or power contact surfaces takes place.

As a result of the separate manufacturing of signal conductor tracks and power conductor tracks, structures with differing heights can be created with relatively simple process steps. The already present signal conductor tracks are covered and except for suitable contact points sealed off for the protection from the process steps to follow. The base material used by means of the most differing processes can be equipped with a negative structure, which predetermines the course of the power conductor tracks. In preference, this structure goes right through to the base carrier, so that thereupon a coating of the base carrier in the zone of the negative structure can take place. For the metallisation taking place, also differing processes can be utilised. The structured layer defines the form of the power conductor tracks and corresponding contact surfaces, which are creatable by the metallisation. Thereafter the structured layer protects the corresponding track - and contract structures during the manufacturing process.

In preference, on the base carrier in the zone of the negative structure a conductive adhesive layer can be deposited, which serves as the base for the metallisation process. It is important, that an adequate connection between the base carrier and the conductor track structures is produced. This preferably can be implemented by a more expensive adhesive layer, which effects the anchoring in a better manner. The

further adhesion is thereupon achievable by means of simple metallisation processes, because the adhesive layer possesses a corresponding conductivity.

Favourably the structured layer can be deposited by means of a photo-lithographic process Very fine structures with very advantageous ratios of height to width can be manufactured by means of such a process. The designing of conductor tracks and contact surfaces in a shape required is achieved in this manner.

In accordance with a variant of the method, the metallisation process can take place by galvanic deposition of metal. In particular in connection with a conductive adhesive layer, on this layer thereupon the desired structure can be created.

In the case of most applications it will be desirable, that in accordance with a variant, following the metallisation process the structured layer is removed.

In the following, examples of embodiments of the invention presented here are explained in more detail on the basis of drawings. These illustrate:

Fig. 1 A first embodiment of an MCM in a perspective view,

Fig. 2 a second embodiment of an MCM in a side view,

Fig. 3 a third embodiment of an MCM in a perspective view and

Fig. 4 a fourth embodiment of an MCM in a perspective view.

The embodiment of an MCM illustrated in Fig. 1 in essence comprises a continuous, plate-shaped base carrier 1, on which very finely structured electrically conductive signal conductor tracks 2 as well as power conductor tracks 5 with a larger cross section are arranged. The signal conductor tracks 2 respectively lead to a signal contact surface 3, which is arranged at the edge of the base carrier 1, with which the signal zone of the MCM makes contact with the outside. Starting out from the signal connection contact surfaces 3, the signal conductor tracks 2 lead to signal contact surfaces 4, which serve for contacting signal semiconductor components 11. These signal semiconductor components 11 can be housed or unhoused chips. In Fig. 1, solely a single signal semiconductor component 11 is depicted. It goes without saying, that the signal zone can be a complicated as required and can be provided with the number of conductor tracks 2 and signal semiconductor components respectively required for the application purposes. The contacting of the signal semiconductor components 11 and the deposition of the signal conductor tracks 2 and of the contact surfaces 3 and 4 is well known. From the signal semiconductor component 11, additional signal conductor tracks or control lines 8 lead to the power zone of the MCM. These control lines 8 are in immediate contact with corresponding power contact surfaces 7. These power contact surfaces 7 are electrically isolated from power contact surfaces 7a, which are connected with the power conductor tracks 5. The power conductor tracks 5 on the edge of the base carrier 1 lead to power connection contact surfaces 6.

The material of the base carrier 1 depending on the application case can consist of fibre-glass reinforced plastic material (construction in the sense of an MCM-D) or of another suitable material (e.g., an electrically insulated metal). In the embodiment

illustrated, the conductor tracks 2, 8 and 5 are respectively arranged in a single layer. A multi-layered arrangement can be provided.

The connection contact surfaces 3 and 6 serve for the electrical connection of the complete MCM with the environment (e.g., motors to be driven, superordinate computers, sensors .....,etc.).

In the illustrated exemplary embodiment, the signal conductor tracks 2 are approx. 5 to 10 micrometers thick and the power conductor tracks approx. 0.6 to 0.7 mm thick. The width of the power conductor tracks is also a multiple of the width of the signal conductor tracks 2. In the depicted exemplary embodiment, the contact surfaces 7, 7a and 6 have the same height as the power conductor tracks 5. Mounted onto the contact surfaces is a power electronics component 12.

Because a large number of signal semiconductor components 11 and/or only individual power electronics components 12 generate relatively high temperatures, great significance has to be attached to a good heat dissipation. For this purpose, in the zones free of conductor tracks 2, 5 and contact surfaces 3, 4, 6, 7, 7a, at least, however, in the power zone, heat conducting elements 9 can be provided. The heat conducting element 9 illustrated in Fig. 1 is arranged between the power contact surfaces 7, 7a and is in a heat conducting contact with the bottom side of the power electronics component 12. For this purpose, the base carrier 1 is breached in such a manner, that the heat conducting element 9 passes through the base carrier 1 and thus makes a good heat dissipation to the reverse side of the base carrier 1 possible. The eduction of the heat then can take place in the most diverse and varied manner.

The control lines 8 in preference consist of the same material as the power contact surfaces 7, so that a tight connection without any interfering interfaces or connections is created. The high density of integration, which is achievable through the arrangement on the base carrier 1, permits previously inconceivable possibilities of the MCM technology.

In preference, the manufacture of these structures is effected in several steps through photo-lithographic processes in combination with galvanic deposition, so that independently of one another the signal zone and the power zone are produced. The free of any interference transition, however, then takes place at the interfaces.

In the following, on the basis of the Fig. 2 a second embodiment of an MCM is explained in more detail. Hereinafter, only the essential differences to the preceding exemplary embodiment are dealt with. For this reason, the same reference numbers designate the same or equivalent components. A corresponding description is transferable.

The second embodiment in accordance with Fig. 2 essentially comprises two great differences. The contact surfaces 3 and 6 are in connection with the reverse side of the base carrier 1, in which conductor track sections not depicted in more detail pass through the base carrier 1 at this point. Through this, on the reverse side contact elevations are produced, which correspondingly take over the task of the connection contact surfaces 3 and 6. By means of the arrangement of the contact elevation 10 on the reverse side of the base carrier 1, these can be designed with the same height, however, with a differing surface area, as a result of which the contacting of the MCM is very much simplified. The contact elevations 10, e.g., can be provided with so-called solder bumps (i.e., with elevations of soldering tin with the shape of

segments of a sphere). In this manner it is assured, that the complete MCM in a single manufacturing step is simultaneously fixed onto a corresponding substrate and is capable of being electrically contacted by it.

The second difference consists of the fact, that on the electronics component 12 a heat sink 13 is positioned, which takes care of a corresponding heat dissipation. In order that this heat sink 13 does not increase the volume of the complete superstructure to too great an extent, it preferably is a body, the cooling structures of which consist of geometrical shapes (walls, columns, pyramids, etc.) with a high aspect ratio, i.e., with a great ratio of structural height to structural width. In this manner it is ensured, that the heat sink 13 in case of a very small overall height (e.g., 0.5 mm) provides a very large cooling surface area (e.g., in the case of a design of the cooling structures as columns 0.4 mm high a cooling surface area of 25 cm3 per 1 cm2 of base surface area).

In the case of superstructures of MCMs of this kind, over and above this there is the possibility of protecting the signal semiconductor components 11 and in particular the power electronics components 12 from mechanical effects from the outside, e.g., in that housings are provided or an encapsulation of the elements is implemented.

Also in the case of the exemplary embodiment explained in the following in accordance with Fig. 3, only the essential differences are dealt with, for which reason the preceding description is made reference to in complement.

Here the power connection contact surfaces 6 have the same height as the signal connection contact surfaces 3. For this purpose, the signal connection contact

surfaces 3 are designed as columns. These too, can be provided with contact elevations 10, so that a uniform height results. The power conductor tracks 5 in this almost have the same height as the power connection contact surfaces 6, while in contrast the power contact surfaces 7 and 7a are less thick. In doing so, however, it is assured, that the overall cross section of the power contact surfaces 7a is adequate for the power transmission. Also the heat conducting element 9 is correspondingly adapted according to the height of the power contact surfaces 7, 7a. The difference in height of the power contact surfaces 7, 7a and of the power conductor tracks 5 is calculated in such a manner, that a countersunk installation of the power electronic components 12 can be implemented. The whole superstructure of the MCM apart from the countersunk installation of the power electronics components also provides the possibility, that it can be installed with its top side facing downwards. In doing so, once again the installation of the connection contact surfaces 3, 6 with the same height alleviates the contacting. By means of this kind of assembly of the complete MCM, a complete protection of the semiconductor components 11, 12 against mechanical damage results, so that these - if at all - only have to be protected against humidity and harmful chemicals with a thin passivation layer.

The heat conducting elements 9 once again pass through the base carrier 1 and are in connection with a heat sink 13, which is located on the reverse side of the base carrier 1. The heat sink 13 in preference once again comprises cooling structures made of geometrical shapes (walls, columns, pyramids, etc.) with a high aspect ratio. Because this type of heat sink 13 makes available an extremely large cooling surface area, the installation with the top side facing downwards does not present the danger of overheating, even if these components are thereupon integrated in closed-off units, because the heat is adequately dissipated to the outside.

Also in the case of the exemplary embodiment in accordance with Fig. 4, only the most significant differences to the preceding exemplary embodiments are dealt with, for which reason here too, reference is made to the description above with respect to structurally identical elements. In the case of this exemplary embodiment, all signal connection contact surfaces 3 and power connection contact surfaces 6 are designed as column contacts at the edge of the base carrier 1. This arrangement corresponds to a standardisation, so that the MCM as an „intelligent power module" can be plugged into bases available on the market as standard components.

In Fig. 4 it is also very clearly evident, that the routing of the power conductor tracks 5 can be designed in any way required, so that the predefined positions of the connection contact surfaces 6 can be reached. The base carrier 1 and the outside connection contact surfaces 3 necessary for the contacting of the whole MCM can be constructed and shaped in such a manner, that the desired standard geometry is provided. The embodiment according to Fig. 4, for example, corresponds to a so-called „chip-carrier" module (PLCC module) with 15 contact points on its edge. In a similar fashion, without any problem PLCCs with 20, 28, ... 84 poles or PGA-compatible superstructures or any other standard superstructures can be made available. In such cases, where the cross sections of the individual standard contacts is not sufficient to conduct the necessary power to the power electronics components 12, several power conductor tracks for one and the same power contact surfaces 7a can be split-up over several power connection contact surfaces 6 designed as standard contacts, so that overall a sufficiently great conductor cross section is obtained.

Claims

1. Multi-chip-module with a base carrier (1), on which at least in some areas signal conductor tracks (2, 8) arranged at least in a single layer and signal contact surfaces (4) are arranged, and with at least one semiconductor component (11) connected with signal conductor tracks (2) and signal contact surfaces (4) operating in the signal range, **characterised in** that additionally on the base carrier (1) at least in some areas power conductor tracks (5) and power contact surfaces (7, 7a) are arranged in at least a single layer, at least one power electronics component (12) operating in the power range is provided, which is connected with at least one power conductor track (5), at least one power contact surface (7, 7a) and at least one signal conductor track (2, 8) and the power conductor tracks (5) have a larger cross section than the signal conductor tracks (2) at least on the basis of greater thickness dimensions.

2. Multi-chip-module in accordance with claim 1, **characterised in** that the at least one signal conductor track (2, 8) leading to a power electronics component (12) essentially seamlessly verges into a power conductor track (5) and/or power contact surface (7).

3. Multi-chip-module according to claim 1 or 2, **characterised in** that the ratio of the height of a power conductor track (5) and/or power contact surface (7, 7a) to the signal conductor track (2,8) and/or signal contact surface (4) is situated within the range of 2 to 300, in preference 120 to 130.

4. Module in accordance with one of the claims 1 to 3, **characterised in** that the ratio of the conductor cross section of a power conductor track (5) and/or power contact surface (7, 7a) to the conductor cross section of a signal conductor track (2, 8) amounts to 2 to 1000, in preference 80 to 400.

5. Module according to one of the claims 1 to 4, **characterised in** that the ratio of height to width of a power conductor track (5) and/or power contact surface (7, 7a) is situated in the range of 0.1 to 10, in preference 1 to 4.

6. Module in accordance with one of the claims 1 to 5, **characterised in** that at least one power conductor track (5) merges into several power contact surfaces (7a) for the common contacting of a power electronics component (12).

7. Module according to one of the claims 1 to 6, **characterised in** that signal connection contact surfaces (3) and power connection contact surfaces (6) are provided for an external connection belonging to them, wherein the signal

connection contact surfaces (3) and the power connection contact surfaces (6) essentially are of the same height.

8. Module in accordance with one of the claims 1 to 7, **characterised in** that signal connection contact surfaces (3) and power connection contact surfaces (6) are arranged on the side of the base carrier (1), which is opposite the semiconductor components (11) and power electronics components (12) (reverse side), wherein the connection contact surfaces (3, 6) are electrically in connection with the opposite side (front side) by means of conductor track sections passing through the base carrier (1).

9. Module according to one of the claims 1 to 8, **characterised in** that the dimension, which results from the height of a power conductor track (5) minus the height of a power contact surface (7a) electrically in connection with this power conductor track (5), is either the same or greater than the height of the power electronics component (12) contacting this power contact surface (7a).

10. Module in accordance with one of the claims 1 to 9, **characterised in** that on the base carrier (1) at least one heat conducting element is jointly arranged, which is in a thermally conducting connection with a power electronics component (12).

11. Module according to claim 10, **characterised in** that the at least one heat conducting element (9) is connected with a heat exchanger device (13).

12. Module in accordance with claim 11, **characterised in** that the heat exchanger device (13) is located on the reverse side of the base carrier (1) and the heat conducting element (9) passes through the base carrier (1).

13. Module according to claim 11 or 12, **characterised in** that the heat exchanger device (13) comprises fine cooling ribs with a ratio of height to width of 0.1 to 10, in preference 1 to 4.

14. Module in accordance with one of the claims 1 to 13, **characterised in** that a heat exchanger device (13) is directly thermally conductively connected with a power electronics component (12).

15. Module according to one of the claims 1 to 14, **characterised in** that the signal connection contact surfaces (3) and the power connection contact surfaces (6) are grouped and arranged on the base carrier (1) in such a manner, that the module is capable of being inserted into a standardised base.

16. Method for the manufacture of a multi-chip-module with the following steps:

Preparation of a base carrier (1) with signal conductor tracks (2, 8) and signal contact surfaces (4),

deposition of a structured layer, by which at least the signal conductor tracks (2) and signal contact surfaces (4) are essentially covered with the exception of connection points and which comprises a negative structure of the power conductor tracks (5) and/or power contact surfaces (7, 7a),

filling-up of the negative structure by means of a metallisation process for the creation of the power conductor tracks (5) and/or power contact surfaces (7), wherein at the connection points a contacting of the signal conductor tracks (2, 8) and/or signal contact surfaces (4) and of the power conductor tracks (5) and/or the power contact surfaces (7) is effected.

17. Method according to claim 16, **characterised in** that a conductive adhesive layer is deposited on the base carrier (1) in the zone of the negative structure, which serves as base for the metallisation process.

18. Method in accordance with claim 16 or 17, **characterised in** that the structured layer is deposited by means of a photo-lithographic process.

19. Method according to one of the claims 16 to 18, **characterised in** that the metallisation process is effected by the galvanic deposition of metal.

20. Method in accordance with claim 19, **characterised in** that following the metallisation process the structured layer is removed.

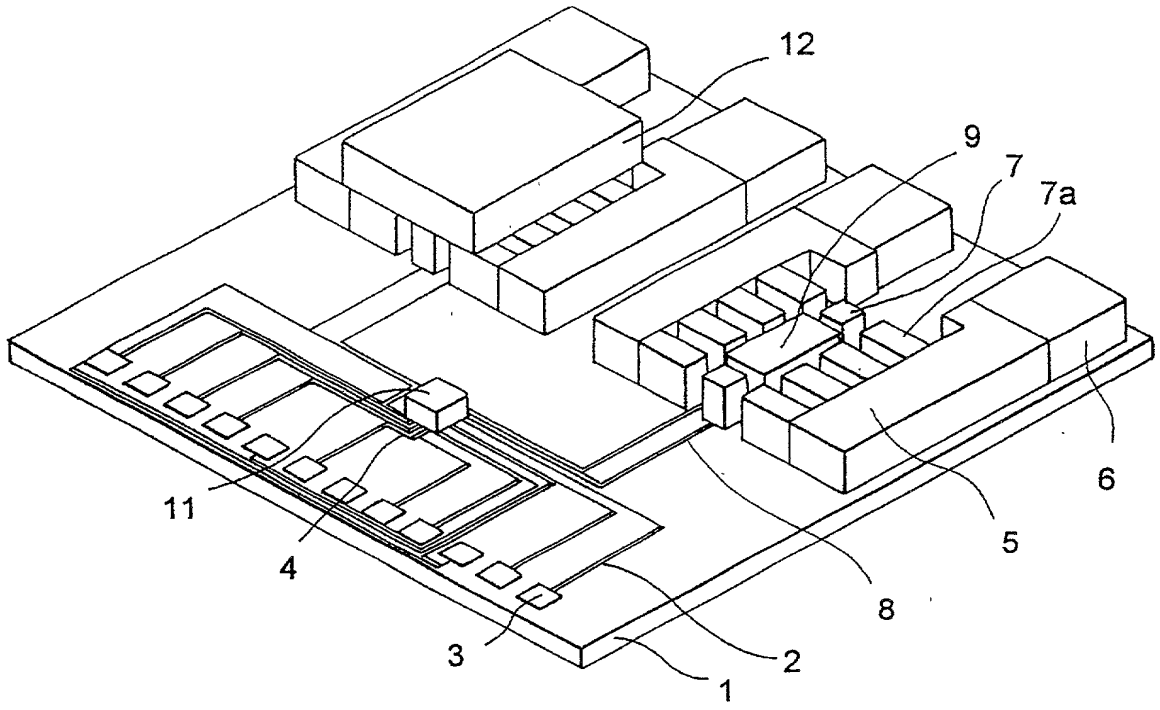

FIG.1

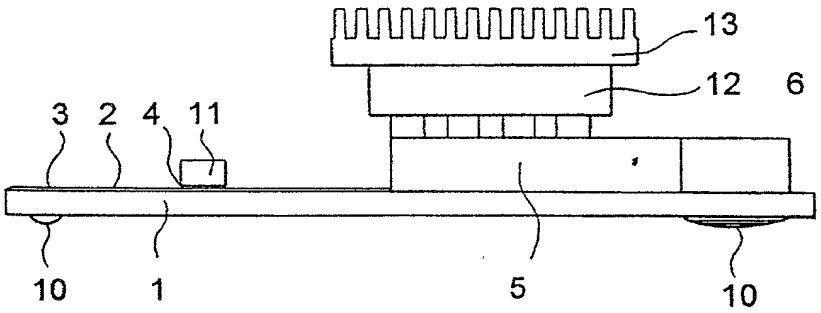

FIG.2

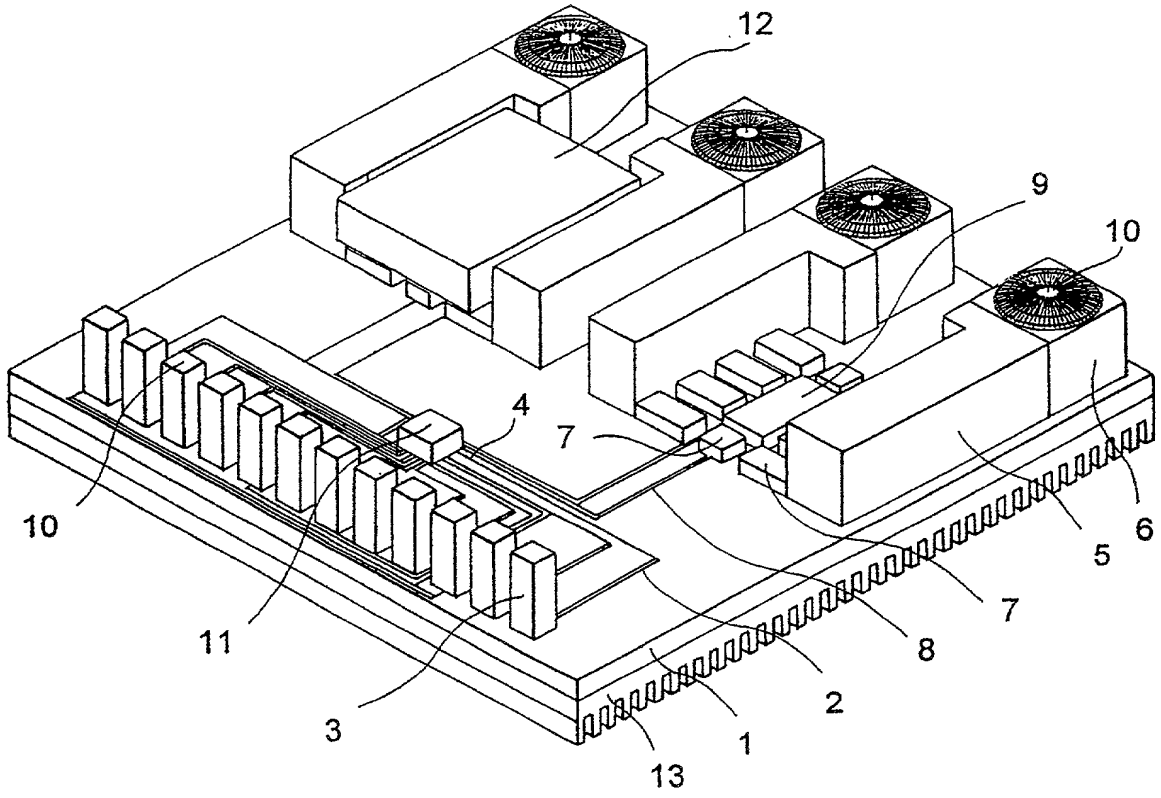

FIG.3

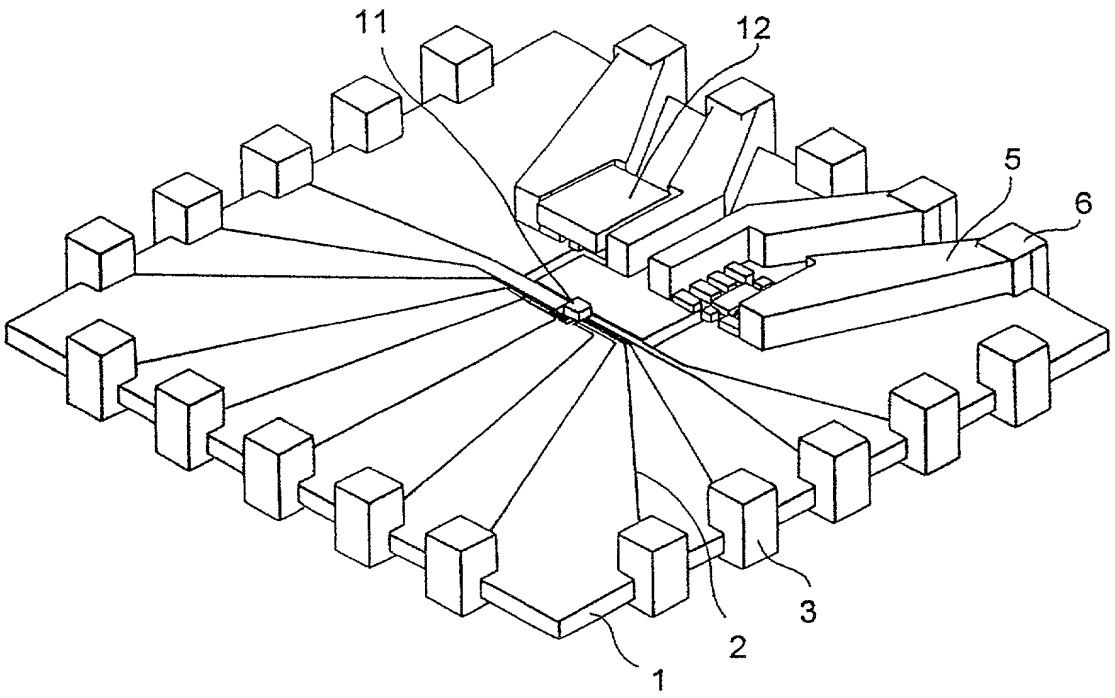

FIG.4

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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

As the below named inventor(s), I/we declare that:

This declaration is directed to:

☐ The attached application, or

☒ Application No. PCT/EP00/02404, filed on 17 March 2000,

☐ as amended on _____(if applicable);

I/we believe that I/we am/are the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought;

I/ we have reviewed and understand the contents of the above-identified application, including the claims, as amended by any amendment specifically referred to above;

I/we acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me/us to be material to patentability as defined in 37 CFR 1.56, including material information which became available between the filing date of the prior application and the National or PCT International filing date of the continuation-in-part application, if applicable; and

All statements made herein of my/own knowledge are true, all statements made herein on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001, and may jeopardize the validity of the application or any patent issuing thereon.

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Signature:		Citizen of:	

☐ Additional inventors are being named on _____additional form(s) attached hereto.

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